

The logo for EPFL (École Polytechnique Fédérale de Lausanne) is displayed in a bold, red, sans-serif font. It consists of the letters 'EPFL' where the 'E' and 'F' are stylized with a grid-like pattern.

Génie Electrique et Electronique
Master Program
Prof. Elison Matioli

EE-557 Semiconductor devices I

Three terminal MOSFET

Outline of the lecture

MOSFET properties

- Device characteristics
- Inversion layer transport and mobility

References:

- J. A. del Alamo, course materials for 6.720J Integrated Microelectronic Devices, Spring 2007. MIT OpenCourseWare (<http://ocw.mit.edu/>)

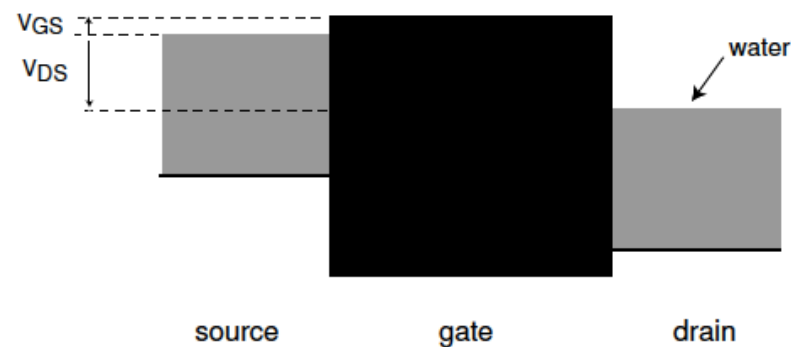
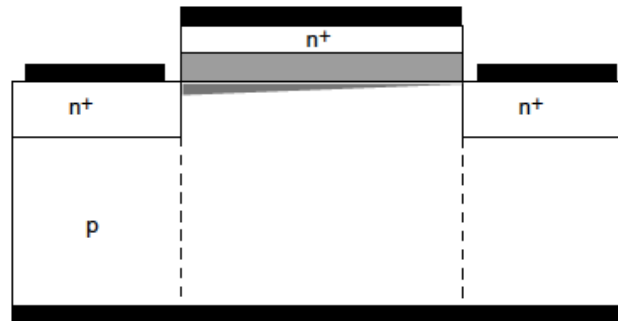
- How does lateral transport through the inversion layer take place?
- What are the most important regimes of operation of a MOSFET?
- What are the key functional dependencies of the MOSFET drain current on the gate and drain voltage?
- Why under some conditions does the drain current saturate?

Qualitative operation of the ideal MOSFET

Useful aspect of MOSFETs: Ability to create an inversion layer independent from the rest of the structure

Water analogy of MOSFET:

- Source: water reservoir
- Drain: water reservoir
- Gate: gate between source and drain reservoirs



We want to understand MOSFET operation as a function of:

- gate-to-source voltage (gate height over source water level)
- drain-to-source voltage (water level difference between reservoirs)

Initially consider source tied up to body (substrate or back).

Qualitative operation of the ideal MOSFET

Three regimes of operation:

Cut-off regime:

- MOSFET: $V_{GS} < V_T$, $V_{GD} < V_T$ with $V_{DS} > 0$.
- Water analogy: gate closed; no water flows regardless of relative height of source and drain.



$$I_D = 0$$

cut-off

Qualitative operation of the ideal MOSFET

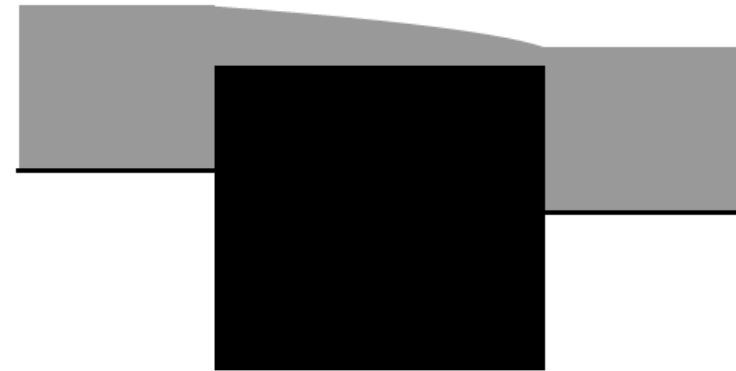
Linear (or Triode) regime:

MOSFET: $V_{GS} > V_T$, $V_{GD} > V_T$, with $V_{DS} > 0$.

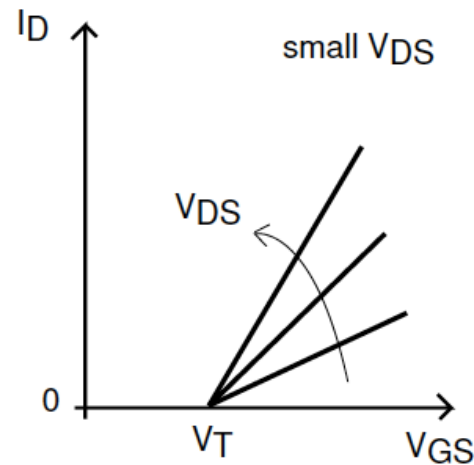
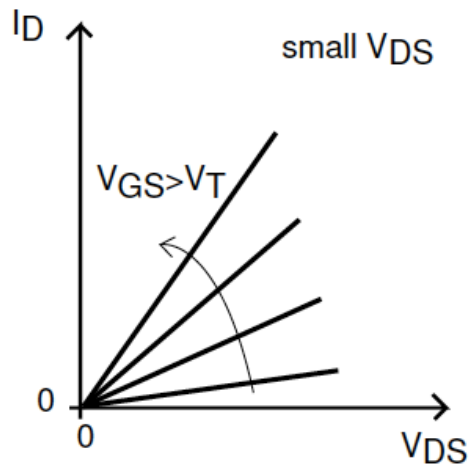
Water analogy: gate open but **small difference in height between source and drain**; water flows.

**Electrons drift from source to drain
⇒ electrical current!**

- $V_{GS} \uparrow \rightarrow |Q_i| \uparrow \rightarrow I_D \uparrow$
- $V_{DS} \uparrow \rightarrow \mathcal{E}_y \uparrow \rightarrow I_D \uparrow$



linear or triode



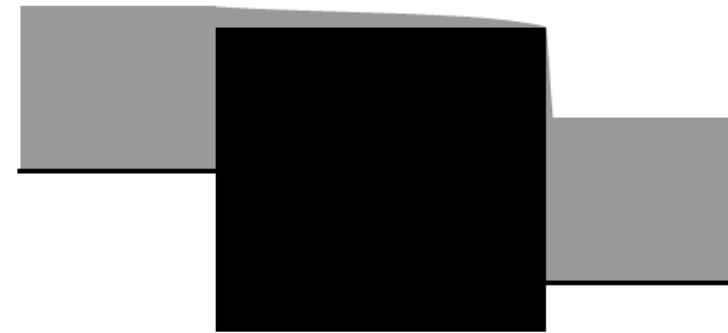
Qualitative operation of the ideal MOSFET

Saturation regime:

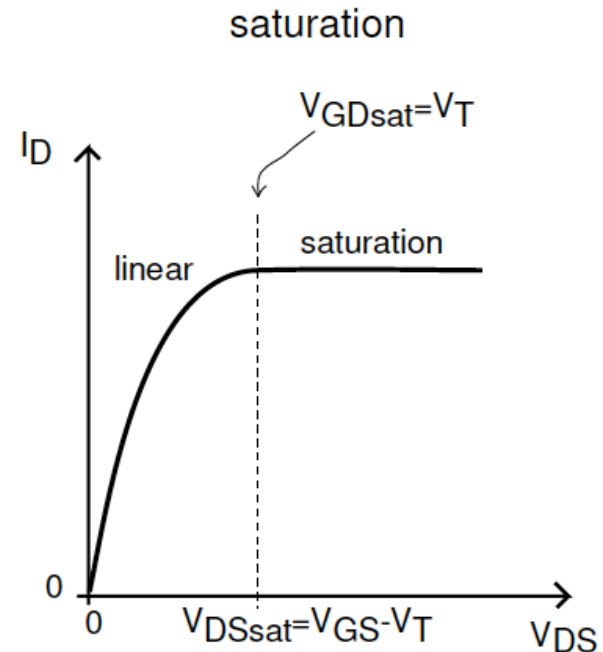
MOSFET: $V_{GS} > V_T$, $V_{GD} < V_T$ ($V_{DS} > 0$).

Water analogy: gate open; water flows from source to drain, but free-drop on drain side
 \Rightarrow total flow independent of relative reservoir height!

Electrons drift from source to drain \Rightarrow electrical current!

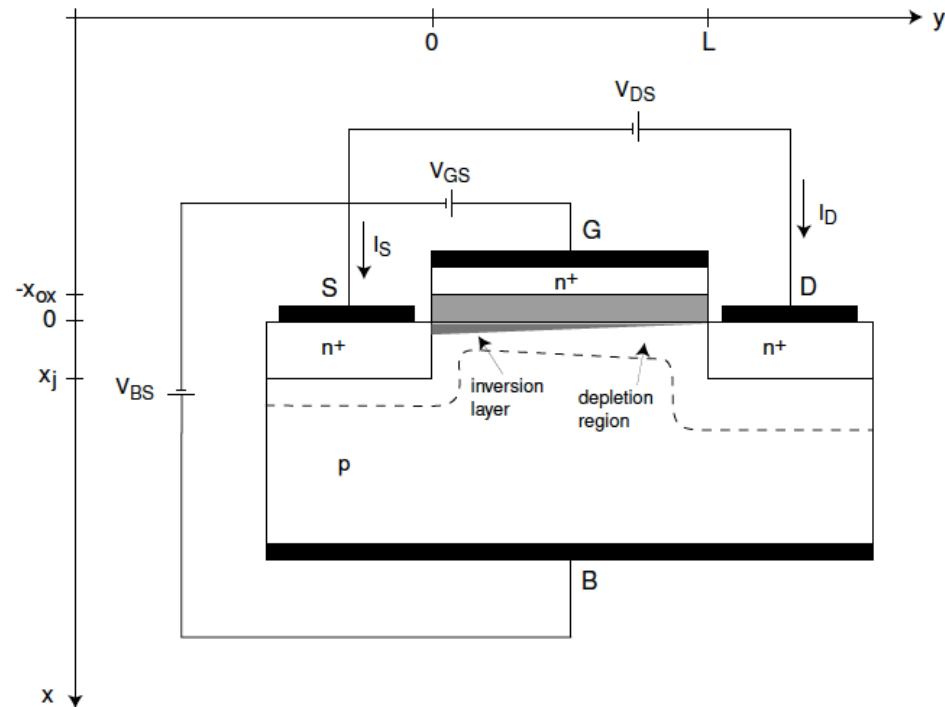


I_D independent of V_{DS} : $I_D = I_{Dsat}$



Inversion layer transport

Want a formalism to describe lateral current along inversion layer.



Sheet charge approximation

Not interested in details of electron distribution in depth (along x).
 Define sheet carrier concentration:

$$n_s(y) = \int_0^\infty n(x, y) dx \quad [cm^{-2}]$$

General expression for inversion layer current:

$$I_e \simeq -qW v_{ey}(y) n_s(y)$$

Note: I_e independent of y .

Inversion layer transport

Define sheet charge density of inversion layer:

$$Q_i(y) = -qn_s(y) \quad [C/cm^2]$$

Thus

$$I_e \simeq Wv_{ey}(y)Q_i(y)$$

This is the sheet charge approximation (SCA)

- It is meaningful to define an average lateral velocity for electrons
- SCA is valid if v_{ey} does not change too rapidly in depth

Under low lateral field:

$$v_{ey}(y) \simeq -\mu_e \mathcal{E}_y(y)$$

Thus

$$I_e \simeq -W\mu_e \mathcal{E}_y(y)Q_i(y)$$

Inversion layer transport

Definition of $V(y)$

$$V(y) = \phi_s(y) - \phi_s(y = 0)$$

The source (located at $y = 0$) is the reference for V

The lateral electric field along the inversion layer is:

$$\mathcal{E}_y(y) = -\left. \frac{dV(y)}{dy} \right|_y$$

Thus:

$$I_e = W \mu_e Q_i(y) \left. \frac{dV(y)}{dy} \right|_y$$

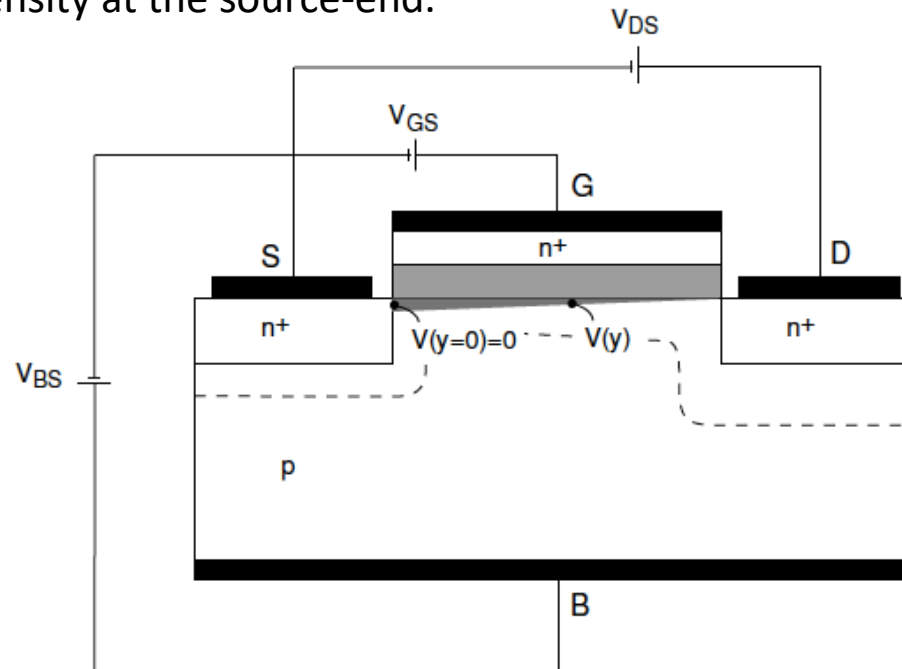
Now we need to relate $Q_i(y)$ with $V(y)$

Inversion layer transport

Remember fundamental **charge-control relationship** for inversion layer in two-terminal MOS structure:

$$Q_i = -C_{ox}(V_G - V_T)$$

In MOSFET, this equation only applies at source end, where $V(0) = 0$.
Thus Q_i is the charge density at the source-end.



For rest of the channel, reuse this relationship accounting for local potential drop:

$$Q_i(y) \simeq -C_{ox}[V_{GS} - V(y) - V_T]$$

Q_i depends on y through local inversion layer voltage $V(y)$.

Inversion layer transport

This is called the **gradual-channel approximation (GCA)**.

GCA allows break up of 2D electrostatics problem into two simpler quasi-1D problems:

- vertical electrostatics control inversion layer charge
- lateral electrostatics control lateral flow of charge.

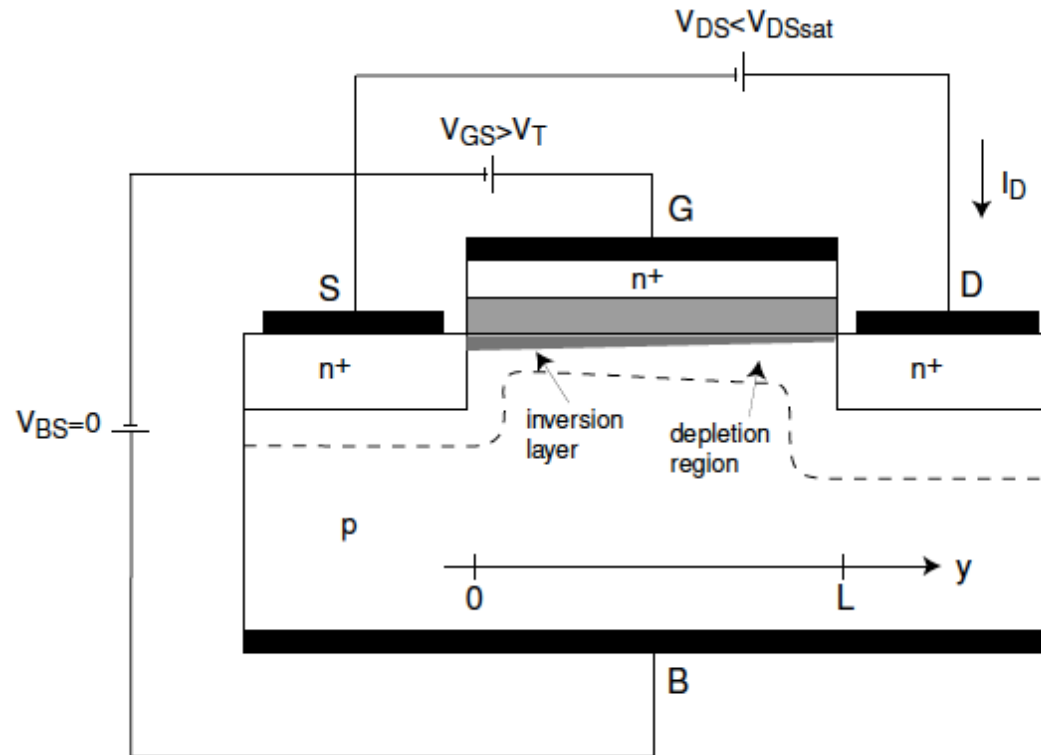
Note: V_T is function of y through body effect

Under GCA, current equation becomes:

$$I_e = -W \mu_e C_{ox} [V_{GS} - V(y) - V_T] \frac{dV(y)}{dy} \Big|_y$$

I-V characteristics of ideal MOSFET

Consider MOSFET in linear regime ($V_{GS} > V_T, V_{GD} > V_T$):



Inversion layer everywhere under gate.

Lateral field set up along channel \rightarrow current flows.

Electrons drift from source to drain \Rightarrow electrical current!

- $V_{GS} \uparrow \rightarrow |Q_i| \uparrow \rightarrow I_D \uparrow$
- $V_{DS} \uparrow \rightarrow \mathcal{E}_y \uparrow \rightarrow I_D \uparrow$

I-V characteristics of ideal MOSFET

Separate variables:

$$I_e dy = -W \mu_e C_{ox} (V_{GS} - V - V_T) dV$$

Integrate from $y = 0$ ($V = 0$) to $y = L$ ($V = V_{DS}$):

$$I_e \int_0^L dy = -W \mu_e C_{ox} \int_0^{V_{DS}} (V_{GS} - V - V_T) dV$$

To get:

$$I_e = -\frac{W}{L} \mu_e C_{ox} (V_{GS} - \frac{1}{2} V_{DS} - V_T) V_{DS}$$

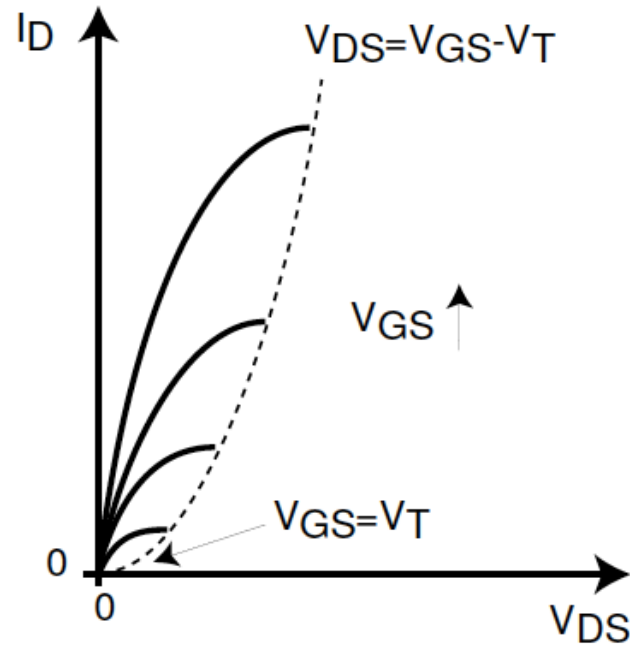
Terminal drain current:

$$I_D = -I_e = \frac{W}{L} \mu_e C_{ox} (V_{GS} - V_T - \frac{1}{2} V_{DS}) V_{DS}$$

Result valid as long as strong inversion prevails in all points of channel. Worst point: $y = L$, for which:

$$Q_i(y = L) = -C_{ox} (V_{GS} - V_{DS} - V_T)$$

Therefore, need $V_{DS} < V_{GS} - V_T$, or $V_{GD} > V_T$.

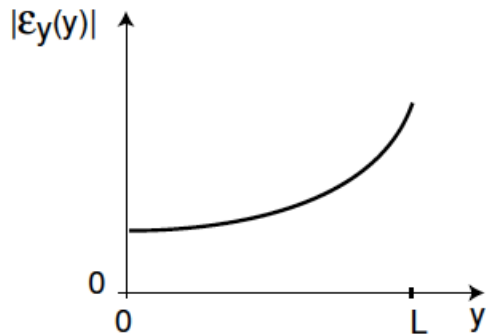
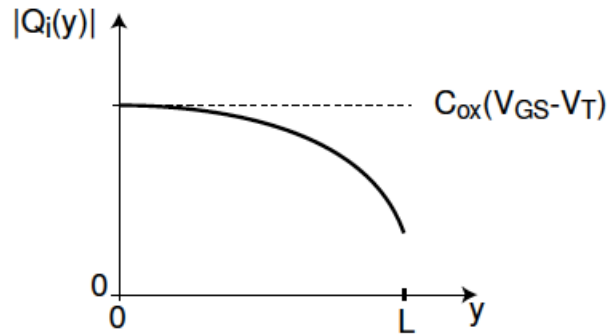


$$I_D = \frac{W}{L} \mu_e C_{ox} (V_{GS} - V_T - \frac{1}{2} V_{DS}) V_{DS}$$

Key dependences of I_D in linear regime:

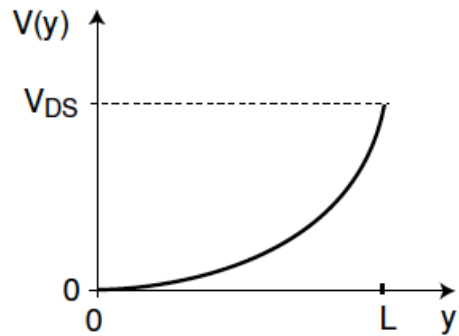
- $V_{DS} = 0 \Rightarrow I_D = 0$ for all V_{GS} .
- For $V_{GS} > V_T$: $V_{DS} \uparrow \Rightarrow I_D \uparrow$ (but eventually I_D saturates).
- For $V_{DS} > 0$ and $V_{GS} > V_T$: $V_{GS} \uparrow \Rightarrow I_D \uparrow$.
- For $V_{GS} = V_T \Rightarrow I_D = 0$

Study lateral electrostatics

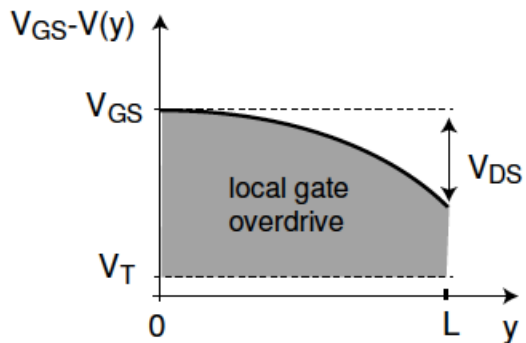


Along channel from source to drain:

$$V \uparrow \Rightarrow V_{GS} - V(y) - V_T \downarrow \Rightarrow |Q_i| \downarrow \Rightarrow |\mathcal{E}_y(x = 0)| \uparrow$$



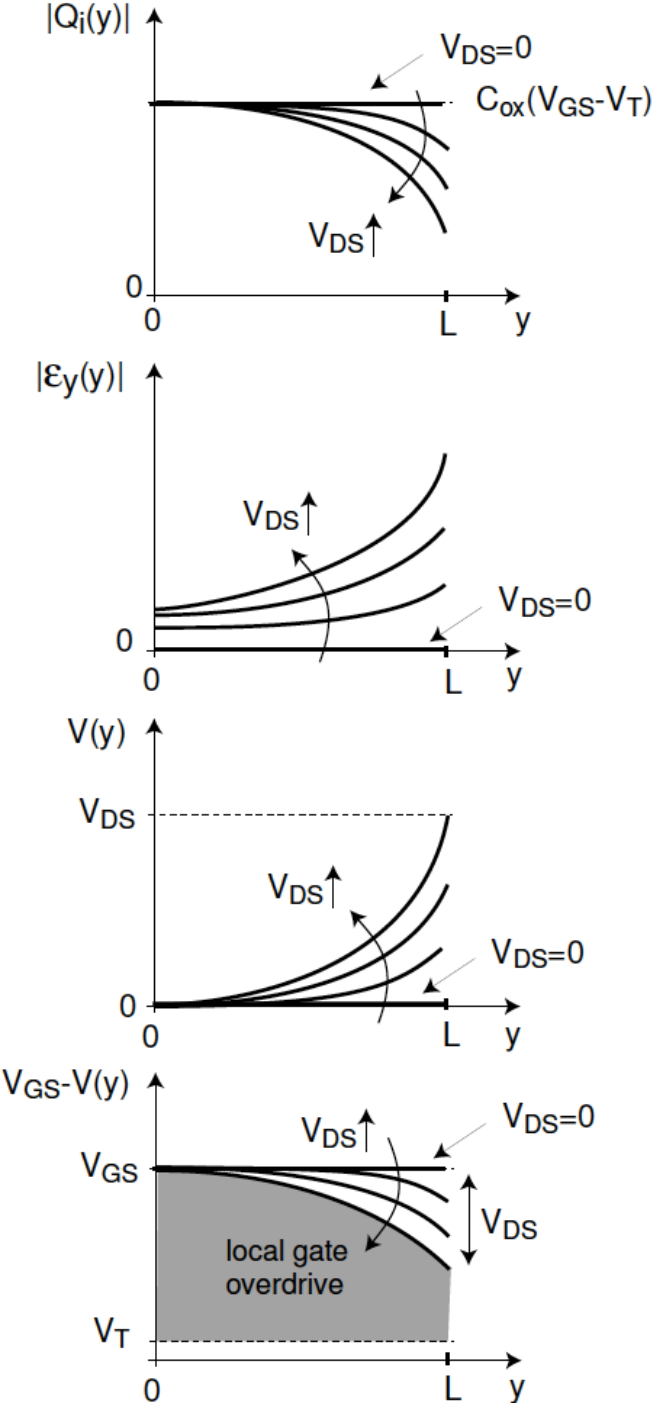
Local overdrive on gate reduces close to the drain.



Study lateral electrostatics

Impact of V_{DS} :

As $V_{DS} \uparrow$ channel debiasing is more prominent.



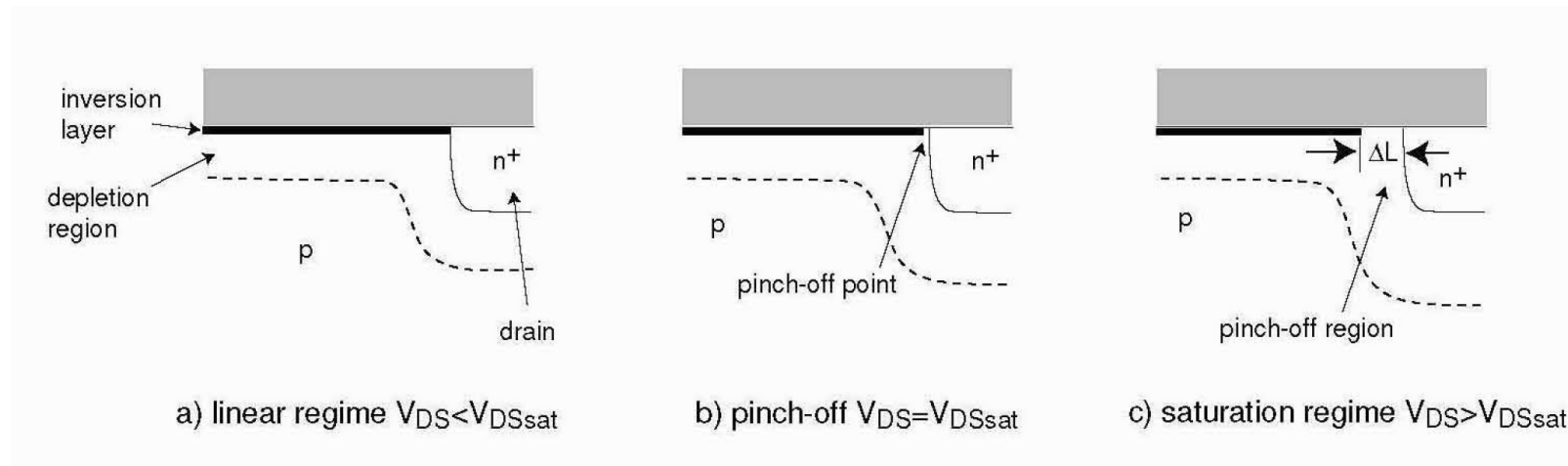
What happens if V_{DS} reaches or exceeds $V_{GS} - V_T$?

Electron concentration at $y = L$ drops to very small concentrations:
depletion region appears at $y = L$: pinch-OFF.

Depletion region is not barrier to electron flow:

Large electric field region.

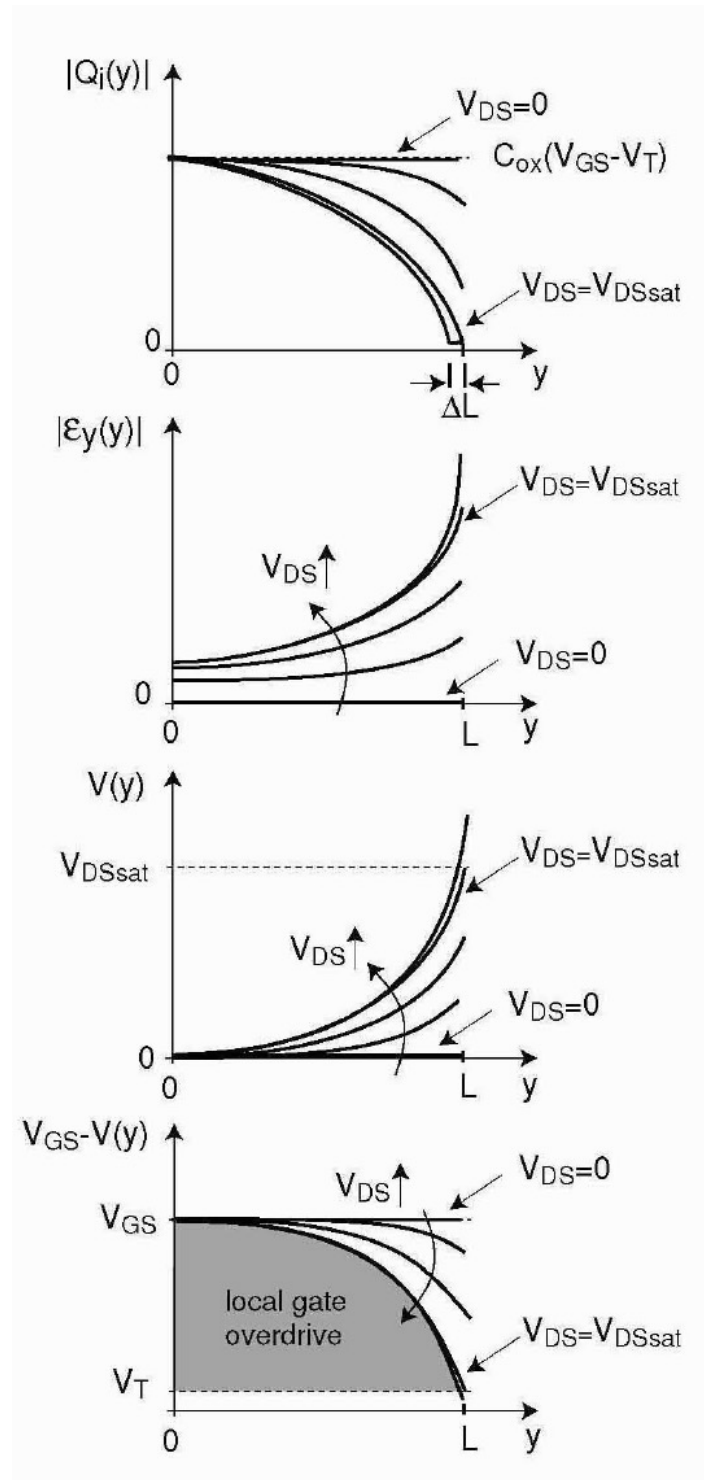
Field "pulls" electrons into drain.



- As V_{DS} exceeds $V_{GS} - V_T$, depletion region widens into channel underneath gate;
- All extra voltage consumed in depletion region;
- Electrostatics of channel, to first order, unperturbed;
- Channel current unchanged: MOSFET in saturation.

Saturation

Lateral electrostatics in saturation:



Saturation

Current model in saturation: I_D does not increase passed $V_{DS} = V_{GS} - V_T$.

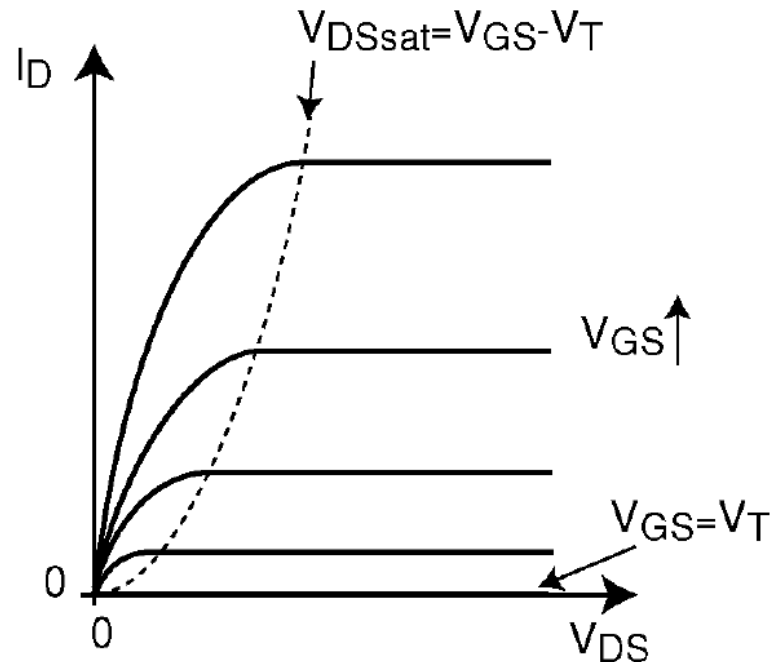
Hence,

$$I_{Dsat} \simeq I_D(V_{DS} = V_{GS} - V_T) \simeq \frac{W}{2L} \mu_e C_{ox} (V_{GS} - V_T)^2$$

V_{DS} at which transistor saturates is denoted as V_{DSsat}

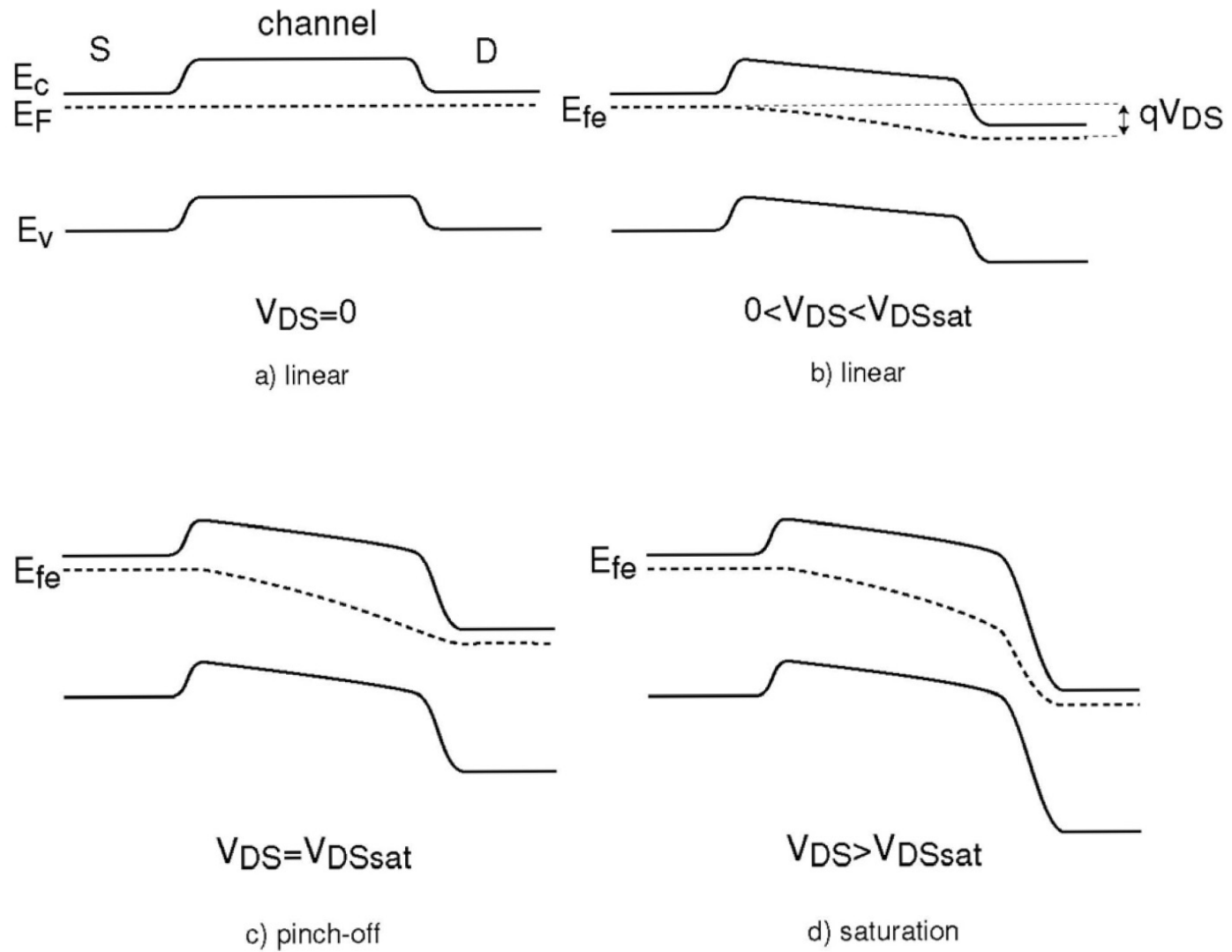
$$V_{DSsat} = V_{GS} - V_T$$

Current-voltage characteristics:



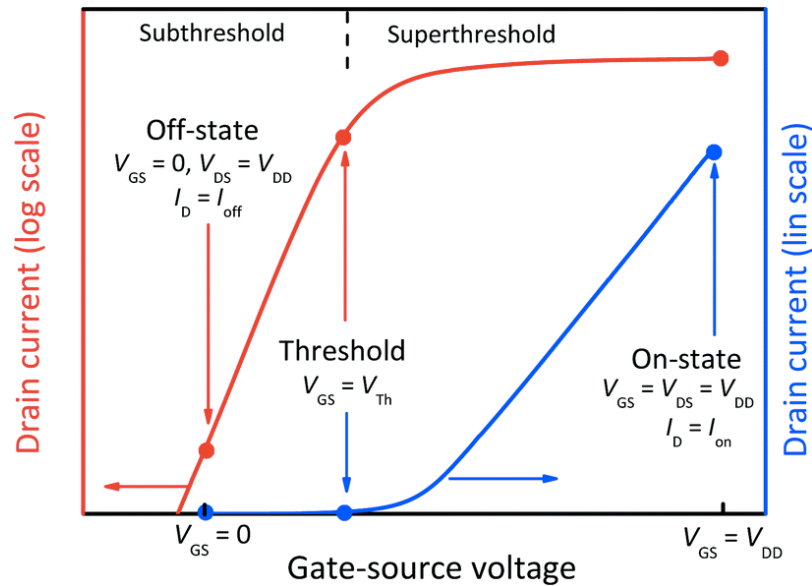
Saturation

Energy band diagrams ($V_{GS} > V_T$):

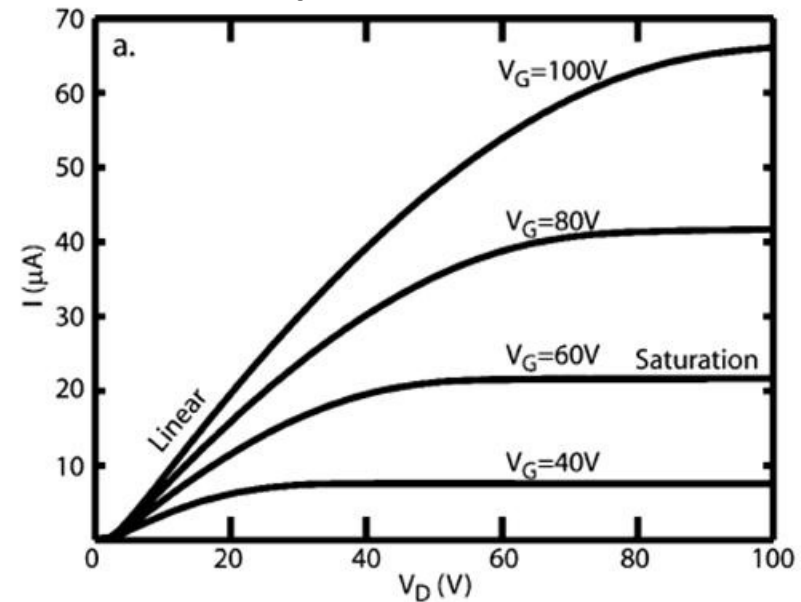


Pinch-off point: region of "free fall" of electrons

Transfer characteristics



Output characteristics



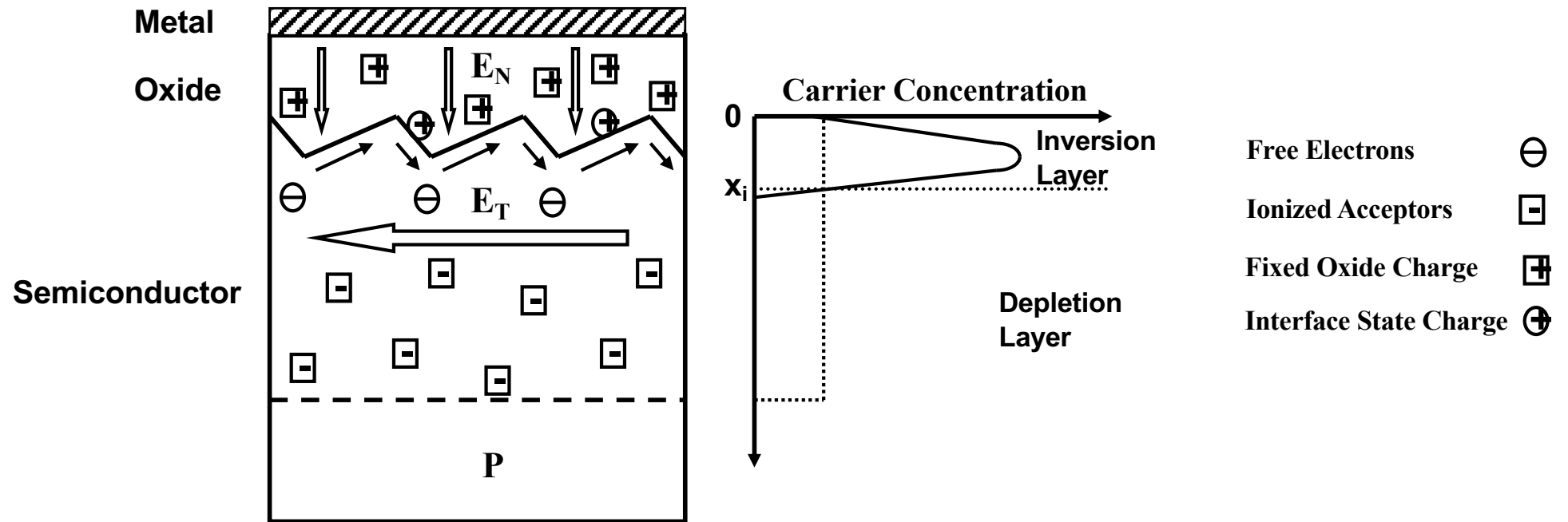
$$I_D = \frac{W}{L} \mu_e C_{ox} (V_{GS} - V_T - \frac{1}{2} V_{DS}) V_{DS}$$

Transconductance

$$\left\{ \begin{array}{l} g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}} = \frac{W}{L} C_{OX} \mu V_{DS} \quad \text{linear} \\ g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}} = \frac{W}{L} C_{OX} \mu (V_{GS} - V_T) \quad \text{saturation} \end{array} \right.$$

Output conductance
(equal to 0 in saturation)

$$g_D = \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}} = \frac{W}{L} C_{OX} \mu (V_{GS} - V_T)$$



Field-Effect Mobility: $\mu_{FE} = \frac{L}{WC_{OX}V_D} \frac{dI_D}{dV_G}$ *From transconductance*

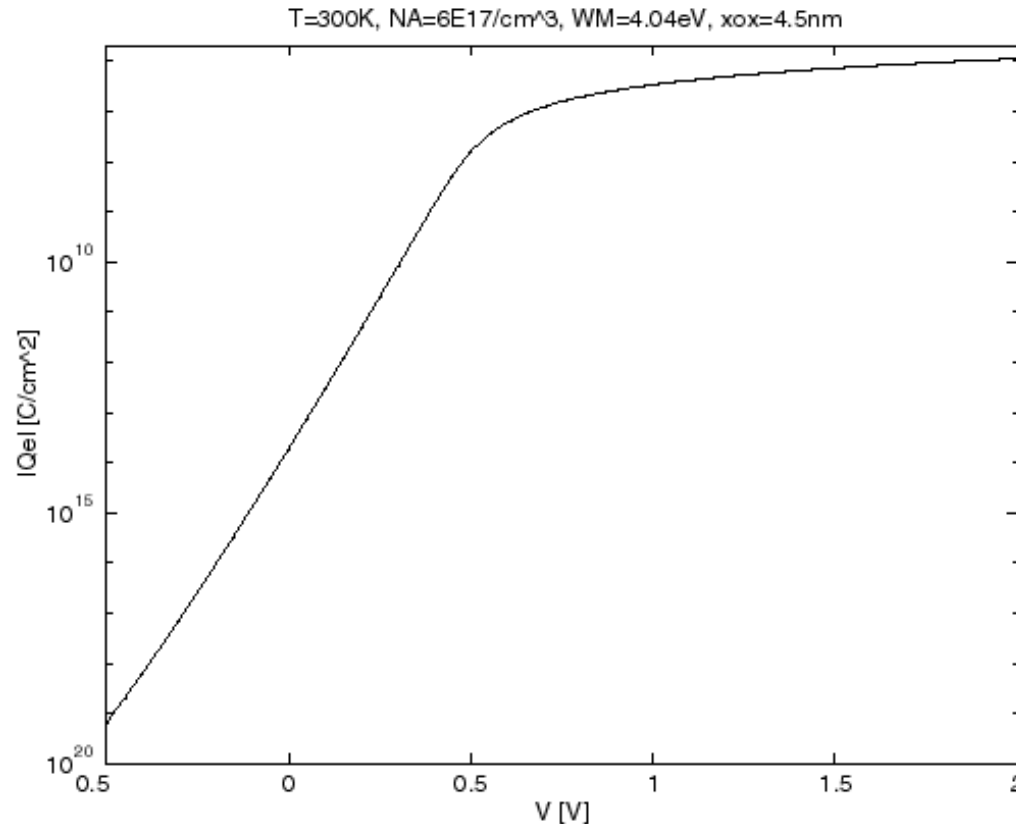
Effective Mobility: $\mu_{EFF} = \frac{L}{WC_{OX}(V_G - V_T)} \frac{dI_D}{dV_D}$ *From output conductance*

Sub-threshold regime

In MOSFETs: current with the device nominally OFF, that is, for $V < V_{th}$:

Sub-threshold current

MOS structure in depletion but finite electron concentration at surface:



Compute Q_e in depletion:

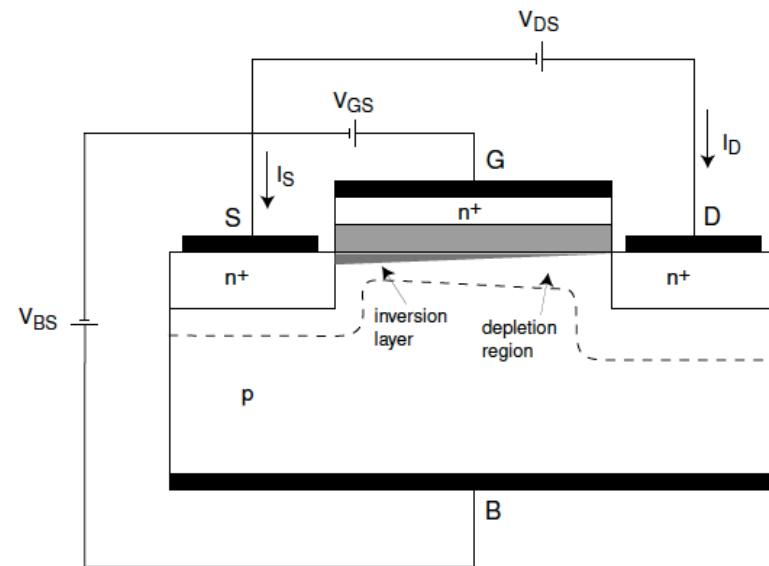
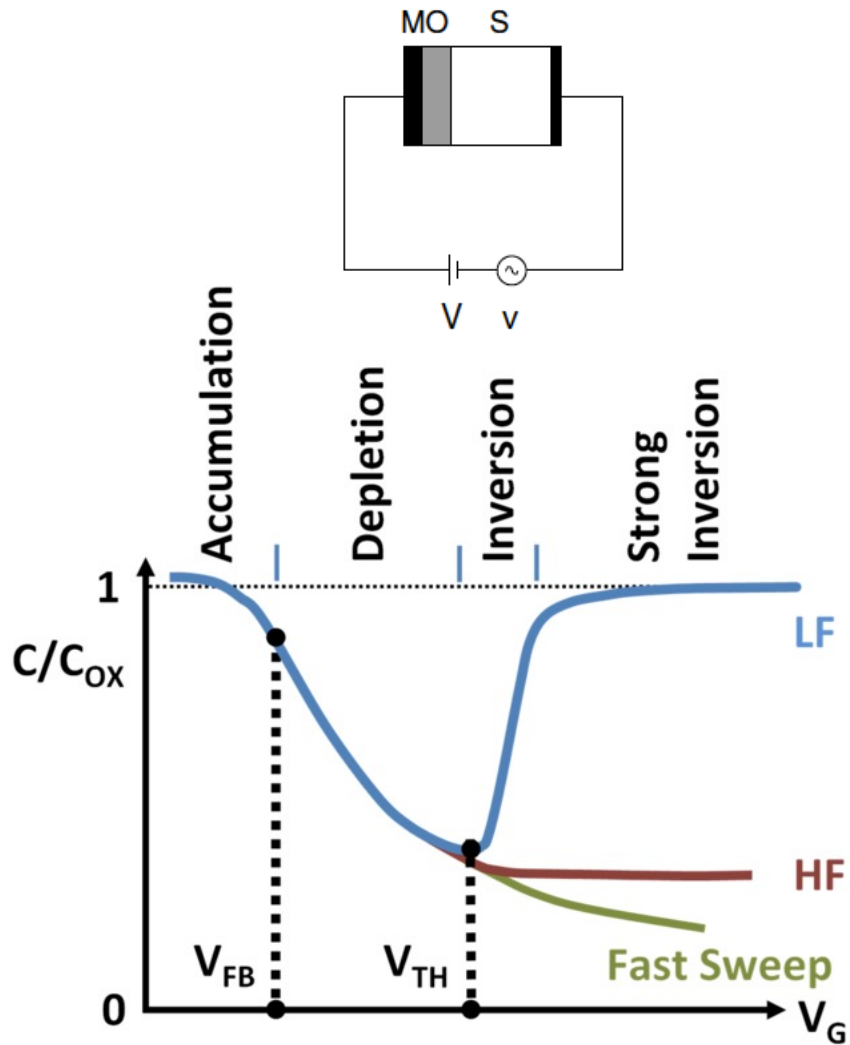
$$Q_e \approx -\frac{kT}{q} \frac{n_i^2}{N_A^2} \sqrt{\frac{q\epsilon_s N_A}{2\phi_s}} \exp\left(\frac{q\phi_s}{kT}\right)$$

Key characteristic of subthreshold regime is inverse subthreshold slope:

$$S = n \frac{kT}{q} \ln 10$$

At best, if $n = 1$, **S = 60 mV/dec** at room temperature. Typically, $S = 80-100$ mV/dec.

The formation of an inversion layer in a MOS structure is very slow. How about in a MOSFET?



The formation of an inversion layer in a MOS structure is very slow. How about in a MOSFET?

In a MOS, the minority carriers characteristic time is defined by generation and recombination, which takes us-ms

In MOSFETs, charge movement into the channel is horizontal, while gate charging is vertical and only creates the field.

These two processes happen simultaneously, but they're very different:

Gate charging (vertical direction):

- Charges flow from the *gate driver* into the gate
- Establishes the electric field through the oxide
- Fast (limited by $R_{gate} \times C_{ox}$)

Inversion charge formation (horizontal direction):

- Electrons flow from the *source/drain* into the surface region, not from the substrate.
- They become “minority carriers” simply because they enter p-type silicon
- Also fast (limited by carrier transport + surface potential rise)

The RC model describes how quickly the **vertical electric field** is established, but the **electrons that fill the inversion layer actually come from the source/drain**, not the gate.

Key conclusions

Sheet-charge approximation: inversion layer very thin in scale of vertical dimensions
 \Rightarrow current formulation in terms of Q_i .

Gradual-channel approximation: electric field changes relatively slowly along channel
 \Rightarrow GCA breaks 2D electrostatics problem into two quasi-1D problems:

- vertical electrostatics control inversion layer charge
- lateral electrostatics control lateral flow of charge

Consequence of GCA: local inversion layer sheet-charge density: $Q_i(y) \simeq -C_{ox}[V_{GS} - V(y) - V_T]$

In **linear regime**, I_D modulated by V_{GS} and V_{DS} :

V_{GS} , to first order, controls electron concentration in channel

V_{DS} , to first order, controls lateral electric field in channel

MOSFET current in **linear regime**:
$$I_D = \frac{W}{L} \mu_e C_{ox} (V_{GS} - V_T - \frac{1}{2} V_{DS}) V_{DS}$$

MOSFET current in **saturation regime**:
$$I_{Dsat} = \frac{W}{2L} \mu_e C_{ox} (V_{GS} - V_T)^2$$

V_{DS} that saturates transistor $V_{DSsat} = V_{GS} - V_T$